

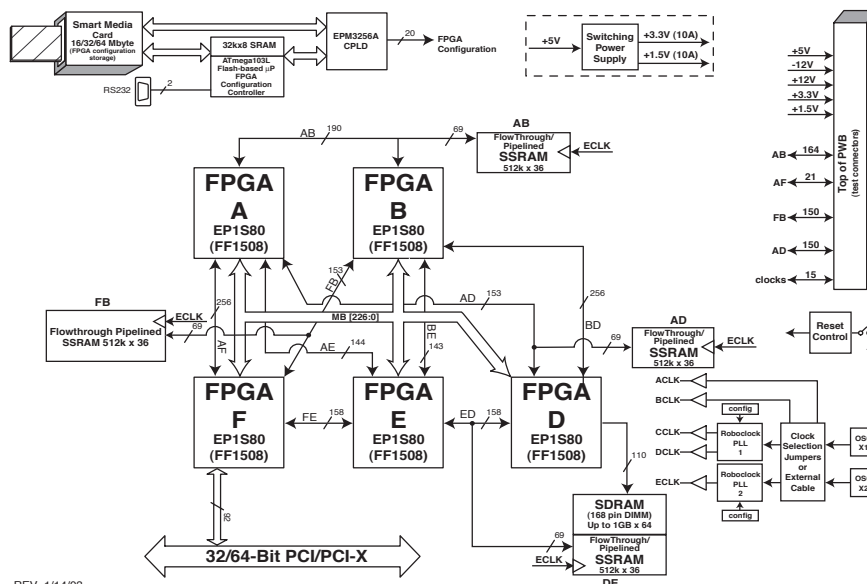
Stratix™-Based ASIC Prototyping Engine

Features

- 32/64 bit, +3.3V PCI/PCI-X-based PWB
- Available in configurations with two to five Stratix™ EP1S80 FPGAs (1508BGA)
- Four external 512k x 36 SSRAMs
 - Pipeline, flowthrough or ZBT
 - Supports up to 2M X 36 SSRAMs
- One external 72-bit SDRAM DIMM
 - Ships standard with a 512 MB SDRAM DIMM (PC133)
 - Supports up to 8 GB SDRAM DIMM
- Tightly interconnected FPGAs facilitate the partitioning process.
- Status LEDs provide instant status and operational feedback.
- Flexible, abundant and configurable embedded memory in FPGAs:
 - 4.6 MB dual-port ESB RAM blocks (assuming five 1S80s)
- Two CY7B993/4 RoboclockII PLLs
- Two FCT3807 Clock Drivers (non-PLL)
- +10 A switching regulator for both +3.3V and +1.5V (only requires +5 V power)
- Standalone operation via separate power connector
- Fast/Easy FPGA configuration via standard SmartMedia FLASH card
 - Microprocessor controlled (ATmega128L)
 - RS232 port for configuration/operational status and control
 - Fastest possible configuration using parallel bus
- Five EP1S80s configure in less than 5 seconds
- Sanity checking programs for bit files simplify the configuration process
- 5 low skew clocks distributed to all FPGAs and headers (from up to 8 possible sources)
 - 2 user-selectable socketed oscillators
 - PCI/PCI-X clock
 - 1 dividable clock via CPLD
 - 4 external clocks via ribbon cable (may be differential!)
- Robust observation/debug with 485+ connections for logic analyzer observability and pattern generator stimulus.
- Custom daughter PWB headers for application-specific circuitry and interfaces.
- Full support for SignalTap and Identify™

Description

The DN5000k10 is a complete logic emulation system that enables ASIC or IP designers to prototype logic and memory designs for a fraction of the cost of other solutions. The DN5000k10 is also applicable to algorithmic acceleration and reconfigurable computing. The DN5000k10 can be hosted in a 32/64 bit PCI/PCI-X slot, or can be used standalone. A single DN5000k10 configured with five EP1S80s can emulate up to 3–4 million gates of logic as measured by LSI (not including memories, multipliers, and DSP functions). High I/O count, 1508-pin, flip-chip BGA packages are employed providing for abundant, fixed interconnect between the FPGAs. A total of 485 test pins are provided on the top of the PWB for logic analyzer-based debugging, or for pattern generator stimulus. Custom daughter cards can be mounted to these connectors as a means of interfacing the DN5000k10 to application-specific circuits. A reference 32-bit PCI target design and test bench is provided (in Verilog/VHDL) at no additional cost.



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