

# !! Important Product Information: Do Not Discard !!



## Product Notice XC2V6000 Devices

Dear Xilinx Customer,

Thank you for your interest in the enclosed Virtex-II devices. We would like you to be aware of the following information that has been updated in the Virtex-II datasheets and the Virtex-II Platform FPGA handbook. This information applies to all XC2V6000 devices with JTAG IDCODE revision code = **0011** (binary). If you have any questions, please contact your Xilinx FAE for assistance.

**\*\*\* New Bitstream Requirement \*\*\*:** please note that a new bitstream is required for both ES and production devices. For ISE/Foundation 4.1i software, this new bitstream will be automatically generated beginning with the release of Service Pack 2. If a different software version is used, please download one of the following tactical patches. The necessary files and installation procedure can be found at the following location:

For software version 3.1i  
<http://support.xilinx.com/techdocs/11805.htm>

For software version 4.1i without Service Pack 2  
<http://support.xilinx.com/techdocs/12326.htm>

Once the patch has been installed, the following environment variable must be set in order to generate the appropriate bitstream: (4.1i software beginning with Service Pack 2 will not require the environmental variable setting)

**PC platform:** set XIL\_BITGEN\_VIRTEX2ES=1  
(done at MS-DOS command prompt or via **Control Panel->System** menu tabs)

**UNIX workstation:** setenv XIL\_BITGEN\_VIRTEX2ES 1

Please make sure that the bitstream generated matches the total configuration bits of the new specification. Implementation of a design with this patch installed will result in generation of a bitstream that is approximately 10% larger than originally specified as shown in the following table. The bitstreams from different software versions are functionally equivalent.

Device	Total Configuration Bits (Original Specification)	Software Version Used	Total Configuration Bits (New Specification)
XC2V6000	19,760,032	Tactical patch above	21,849,568
		Beginning with Service Pack 2	21,849,504

Note that the larger bitstream size must be accounted for when selecting SPROM densities to use with these devices.

- 1. DCM Frequency Synthesis operation** – the operating range of the Frequency Synthesis function of the DCM is updated in the Virtex-II datasheets and as follows:

Mode	CLKIN Freq. Range (MHz)	M range	D range	CLKFX Freq (MHz)	
				Min	Max
LF	1 – 200	2 to 32	1 to 32	24	200
HF	50 – 320	2 to 32	1 to 32	200	320

- 2. Configuration in Non-Contiguous Data Strobe Mode** – the Non-Contiguous Data Strobe Mode within the Slave SelectMAP programming mode is updated in the new revision of the Virtex-II Platform FPGA handbook. In order to successfully configure in the Non-Contiguous Data Strobe mode, the setup times of the CS\_B and RDWR\_B signals must be greater than 7ns before the rising edge of CCLK. Additionally, the CS\_B and RDWR\_B signals must be held until the falling edge of CCLK with 0 or positive hold times with respect to the falling edge.
- 3. Bitstream Encryption** – due to the nature of the extended bitstream requirement mentioned above, implementing Triple DES Bitstream Encryption will require careful system and device management during configuration. If an incorrectly keyed bitstream is loaded into the FPGA (i. e., wrong keys or no keys are programmed into the device), the device could draw an excessive amount of current. This could result in the device getting hot and becoming permanently damaged. Please contact your Xilinx FAE for further details.
- 4. Partial Reconfiguration** – the enclosed devices support “active” partial reconfiguration but not “shutdown” partial reconfiguration mode. “Active” partial reconfiguration will be enabled beginning with the 4.2i software release.