

!! Important Product Information: Do Not Discard !!



Engineering Sample Errata Sheet

XC2V6000 ES Devices

Dear Xilinx Customer,

Thank you for your interest in the enclosed Virtex-II Engineering Sample (ES) devices. Although Xilinx has made every effort to ensure that these devices are of the highest possible quality, they are subject to the limitations described in the ES Errata List below. Please review this list to ensure that the enclosed units will meet the requirements of your application.

All Errata List items apply to XC2V6000 ES devices (in all package types) with JTAG IDCODE revision code = **0010** (binary). For additional clarification on the Errata List items or help with related implementation issues, please contact your Xilinx FAE for assistance.

ESD guidelines: the Xilinx guideline for ESD performance of ES devices is 750V / Human Body Model (HBM). The enclosed samples meet this guideline for all primary ESD test conditions. Testing of additional conditions is in progress. Please exercise standard ESD handling precautions with this material at all times.

Mounting guidelines: please refer to the label on the device packaging to ensure that the enclosed samples are mounted in accordance with the listed Moisture Sensitivity Level under EIA JEDEC Standard J-STD-020-A.

***** Software Patch Requirement ***:** please note that a software patch is required in order to generate a bitstream that is compatible with these ES devices. The software patch download and installation procedure can be found at the following location:

<http://support.xilinx.com/techdocs/11805.htm>

Once the patch has been installed, the following environment variable must be set in order to generate the appropriate bitstream:

PC platform: set XIL_BITGEN_VIRTEX2ES=1
(done at MS-DOS command prompt or via **Control Panel->System** menu tabs)

UNIX workstation: setenv XIL_BITGEN_VIRTEX2ES 1

Implementation of a design with this patch installed will result in generation of a bitstream that is approximately 10% larger than originally specified as shown in the following table:

Device	Total Configuration Bits (Original Specification)	Total Configuration Bits (New ES Specification)
XC2V6000	19,760,032	21,849,504

Note that the larger bitstream size must be accounted for when selecting SPROM densities to use with these ES devices. The 2V6000 production devices will not require this extended bitstream, but will be compatible with it in the event that regenerating the bitstream for production units is not an acceptable option to the user.

Virtex-II ES Errata List

1. **Device Operating Conditions** – the recommended operating conditions on the Vccint supply for the enclosed ES devices are:

Parameter	Min	Max
Vccint	1.45V	1.575V

2. **Power Supply Sequencing** – Xilinx recommends that all device power supplies (Vccint, Vcco, Vccaux) be powered up simultaneously. Other power supply sequencing options may result in higher than typical power-up current.
3. **JTAG “Secure” to “Non-Secure” mode switch** – when an encrypted bitstream has been downloaded to the device, switching from Secure to Non-Secure mode via JTAG will cause any subsequent readback operation to capture all zeros. This specific sequence of events may also result in high current consumption due to the resulting contention within the device and should therefore be avoided.
4. **DCM Reset requirement** – Reset the instantiated DCM 0.5sec after DONE signal asserts. This is necessary to ensure proper locking behavior. Do not use the STARTUP_WAIT feature of the DCM. If a non-default configuration startup sequence is being specified, do not use the “LCK_cycle” option..
5. **DCM Fine Phase Shift operation** – the “variable” shift mode of the DCM Fine Phase Shift feature is not available in these devices. “Fixed” shift mode operation is available for use.
6. **DCM Frequency Synthesis operation** – the operation of the Frequency Synthesis function of the DCM has been verified on initial silicon under the following conditions:

Mode	CLKIN Freq. Range (MHz)	CLKFB connection required?	M range	D range	M/D max ratio	CLKFX Freq (MHz)	
						Min	Max
Low Freq	24 – 60	Yes *	2 to 64	1 to 32	2	24	120
	60 - 240	Don't Care	2 to 64	1 to 32	4	24	240

* Note that the CLKFB input to the DCM must be connected for CLKIN frequencies below 60 MHz.

** Measurement operating conditions: Room Temp, Vcc=1.5V.

Functionality outside of these conditions (including operation in High Freq mode) has not been verified at this time, and it is therefore recommended that the enclosed ES devices be operated within the ranges and conditions specified.

7. **DCM CLKDV output behavior** – in very isolated cases, the CLKDV output of the DCM may become permanently stuck in a High or Low state during the locking process. The

likelihood of such an event occurring is extremely low, and there is no risk of the CLKDV output becoming stuck after the locking process is completed.

8. **Digital Spread Spectrum technology** – the actual benefit achieved through use of the DCM spread spectrum feature is application and frequency dependent.
9. **Global Clock Network** – for certain applications that require the cascading of global clock muxes, implementation assistance from a Xilinx FAE may be necessary.
10. **HSTL and GTL standards on input pins** – applications using these standards will require an environment variable setting for the BITGEN software utility. Contact your Xilinx FAE for the proper environment variable setting.
11. **Readback of Configuration Data** – configuration readback is not supported on these devices.
12. **Security Bitgen Option** – level 1 and level 2 configuration security options are not supported. Use only the default “None” setting. A non-default setting will prevent device start-up.
13. **Bitstream Encryption and Power-down Mode** – due to the nature of the extended bitstream software patch mentioned above, the enclosed ES devices do not support the Bitstream Encryption or Power-down Mode functions. Production devices used in conjunction with a standard-sized bitstream will support these functions.
14. **Configuration in Non-Contiguous Data Strobe Mode** – To successfully configure, the setup times of CS_B and RDWR_B must be greater than 7ns before the rising edge of CCLK. Additionally, the CS_B and RDWR_B signals must be held until the falling edge of CCLK with 0 or positive hold times with respect to the falling edge.
15. **IBUFG and DCM placement** – when using software version 4.1i or greater with the enclosed samples, an IBUFG and any connected DCM must be constrained (via the constraints file) to be in the same quadrant for proper functionality. No warning will be given if IBUFG and the connected DCM are in different quadrants.